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Voltage-Controlled Ring Oscillators Based on Inkjet Printed Carbon Nanotubes and Zinc Tin Oxide

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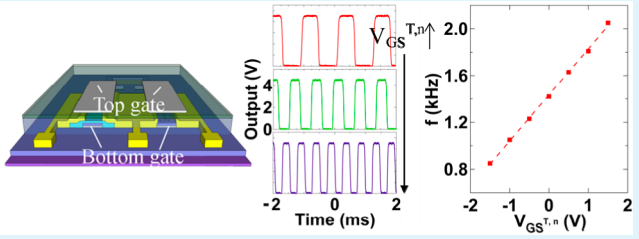
Supporting Information

ABSTRACT: A voltage-controlled ring oscillator is implemented with double-gate complementary transistors where both the n- and p-channel semiconductors are deposited by inkjet printing. Top gates added to transistors in conventional ring oscillator circuits control not only threshold voltages of the constituent transistors but also the oscillation frequencies of the ring oscillators. The oscillation frequency increases or decreases linearly with applied top gate potential. The field-effect transistor materials system that yields such linear behavior has not been previously reported. In this work, we demonstrate details of a material system (gate insulator, p- and n-channel semiconductors) that results in very linear frequency changes with control gate potential. Our use of a double layer top dielectric consisting of a combination of solution processed P(VDF-TrFE) and Al_2O_3 deposited by atomic layer deposition leads to low operating voltages and near-optimal device characteristics from a circuit standpoint. Such functional blocks will enable the realization of printed voltage-controlled oscillator-based analog-to-digital converters.



KEYWORDS: *printed electronics, thin-film transistor, carbon nanotube, zinc tin oxide, double-gate, threshold voltage, voltage-controlled oscillator*

INTRODUCTION

One of the important application area for printed electronics is in sensor systems.[1,2] In such systems, shown schematically as a block diagram in Figure 1, typically weak signals from a sensor are first amplified and then converted to digital form before being transmitted to external electronics. Thus, analog-to-digital signal conversion is a key functional block for printed electronics. Voltage-controlled oscillators (VCOs) are key components of VCO-based analog-to-digital converters (ADCs).[3,4] There have been a few reports on organic-transistor-based ADCs;[5−9] however, most of these were not based on printed semiconductors. In this paper, we report the realization of voltage-controlled double-gate complementary ring oscillators (ROSCs) utilizing inkjet printed semiconductors.

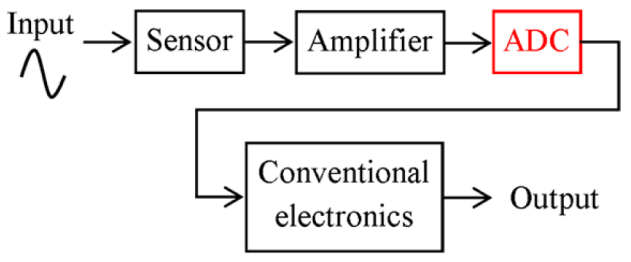


Figure 1. Schematic block diagram of a sensor system.

Numerous semiconductor and dielectric material systems are being investigated for printed electronics. Semiconductor materials such as polymers, amorphous oxides, and single-walled carbon nanotubes (SWCNTs) have been demonstrated in printed electronics with each material possessing advantages and drawbacks for specific applications.[10−15] In previous work, we demonstrated complementary circuits with inkjet printed p-channel SWCNT thin-film transistors (TFTs) and n-channel amorphous oxide TFTs as foundational elements for printed electronics.[16,17] In this paper, we show that the addition of double-gate functionality yields VCOs that are more easily implemented with printed transistors compared to traditional designs based on analog components such as operational amplifiers. Frequency tuning characteristics of double-gate ROSCs with a pentacene active layer have been previously reported.[18,19] However, their use in ADCs and the linearity of tuning characteristics have not received adequate attention and can be improved by using different semiconductors. The response of an ADC is governed by its bandwidth that is

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determined by the sampling rate. For systems such as those depicted in Figure 1, it is not necessary to implement a full ADC at the site of a sensor; rather, the focus should be on keeping the sampling rate as high as possible. This goal is best achieved with voltage-controlled ring oscillators (VCROs) that possess higher oscillation frequencies than the clock frequency of the corresponding digital circuits. Thus, a scheme in which the analog signal is converted to a frequency modulated square wave will efficiently propagate the signal from the sensor to the control electronics, where additional processing can be performed. Adding a buffer amplifier (i.e., two inverters in series) will improve the pulse shape of the VCO output, if required.

EXPERIMENTAL SECTION

Device Fabrication. The bottom gate electrodes, which consist of patterned e-beam evaporated Ti/Pt bilayers (3 nm/30 nm), were formed on Si/SiO_2 substrates by photolithography, followed by lift-off. The bottom gate dielectric layer, ZrO_2, was deposited by a sol–gel route. Via holes to the bottom gate electrodes were patterned by photolithography and reactive ion etching (CHF_3/O_2 at a pressure of 40 mTorr). The n-type active layer, zinc tin oxide (ZTO), was deposited by sequential inkjet printing three times, after UV O_3 surface treatment for 10 min. After ZTO printing, the substrate was annealed on a hot plate at 500 °C for 1 h in air. The p-type active layer, SWCNTs (>98% semiconducting purity prepared by density gradient ultracentrifugation),[20,21] was deposited by inkjet printing, after UV O_3 surface treatment for 10 min. After printing the SWCNTs, the substrate was placed on a hot plate at 200 °C for 30 min in air to remove residual solvents. More details on the preparation of ZrO_2, ZTO, and SWCNT solutions and the printing conditions are described in our previous papers.[16,22−24] The source/drain (S/D) electrodes were patterned by photolithography, and Ti/Au (3.5 nm/20 nm) was deposited by thermal evaporation, followed by lift-off.

Poly(vinylidene fluoride-trifluoroethylene) (P(VDF-TrFE)) (Solvay Solexis Inc., 75/25 mol %) solution, dissolved in diethyl carbonate (25 mg/mL), was spin-coated on top of the devices at a spin speed of 2000 rpm for 45 s. The substrate was baked on a hot plate at 140 °C for 3 min in air to remove solvents. A thin Al_2O_3 layer (12.5 nm) was deposited on top of the P(VDF-TrFE) layer by atomic layer deposition (ALD) at 80 °C. After Al_2O_3 deposition, the top gate dielectrics on the contact pads were removed with acetone. Finally, Ni (50 nm) was deposited by thermal evaporation through a shadow mask to form the top gate electrodes.[25]

Electrical Characterization of Devices. All measurements were performed under ambient conditions. The characteristics of TFTs and inverters were measured using a HP 4155C semiconductor parameter analyzer. For the ROSC measurement, the output signals were measured with a LeCroy WaveRunner 6030 oscilloscope, and other voltages were supplied by the HP4155C.

RESULTS AND DISCUSSION

Figure 2 illustrates a schematic structure of the double-gate complementary inverter based on inkjet printed SWCNTs and ZTO. The top gate dielectric for these devices consists of a bilayer of P(VDF-TrFE) and Al_2O_3. The P(VDF-TrFE) layer has been shown in previous work to mitigate the effects of charged defects in the p-channel SWCNTs, leading to significantly improved electrical characteristics.[26] A thin Al_2O_3 layer was deposited on top of the P(VDF-TrFE) to reduce gate leakage current and improve the overall gate dielectric stack performance.

The threshold voltage (V_{th}) of the TFTs in a double-gate structure can be controlled by the potential applied to either the bottom or top gates.[27−31] In this work, bottom gates were

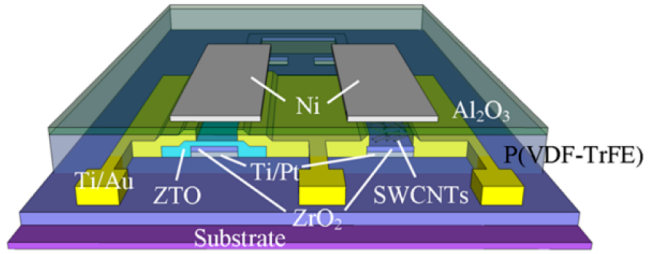

Figure 2. Schematic structure of a double-gate complementary inverter based on inkjet printed SWCNTs and ZTO.

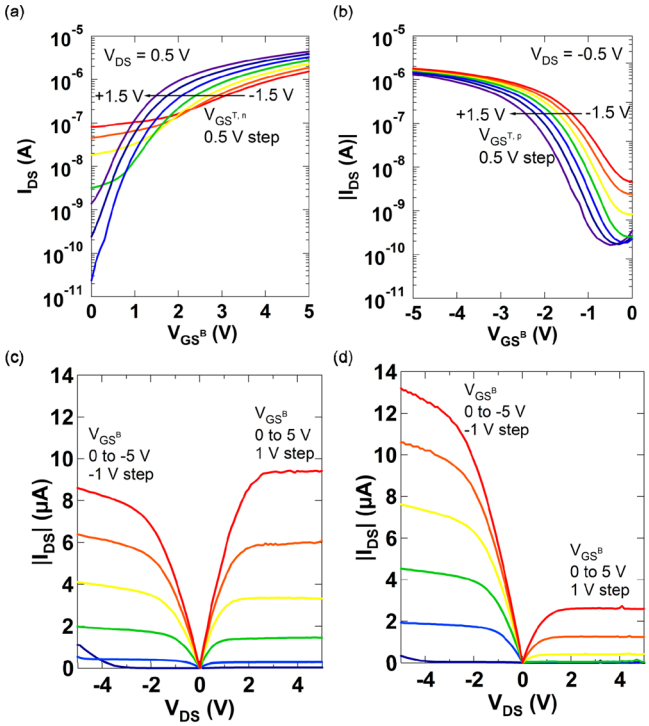

Figure 3. (a) Transfer characteristics of the double-gate ZTO TFT at various n-TFT top-gate-source voltages ($V_{GS}^{T,n}$). (b) Transfer characteristics of the double-gate SWCNT TFT at various p-TFT top-gate-source voltages ($V_{GS}^{T,p}$). (c) Output characteristics of the double-gate SWCNT (left) and ZTO (right) TFTs at V_{GS}^{T} = 1.5 V and at (d) V_{GS}^{T} = −1.5 V.

employed as conventional gates (as in single gate TFTs) because the bottom gate dielectric exhibits a higher capacitance value (148 nF cm^{-2})[16] than that of the top gate dielectric (~106 nF cm^{-2}) (Supporting Information, Figure S1), while the top gates were employed as the control gates. Figure 3a, b shows transfer characteristics of the double-gate TFTs in linear mode ($|V_{DS}|$ = 0.5 V). Both ZTO and SWCNT TFTs possess the same channel length (L) = 20 μm and channel width (W) = 400 μm. The ZTO TFT exhibits linear field-effect mobility of 0.7 cm^2 V^{-1} s^{-1} and an I_{on}/I_{off} ratio of 8.5 × 10^2, while the SWCNT TFT exhibits linear field-effect mobility of 0.3 cm^2 V^{-1} s^{-1} and an I_{on}/I_{off} ratio of 6.2 × 10^3, when the n-TFT top-gate-source voltage ($V_{GS}^{T,n}$) and the p-TFT top-gate-source voltage ($V_{GS}^{T,p}$) are 0 V and $|V_{DS}|$= 0.5 V. In the case of the ZTO TFT, V_{th} shifts toward more negative voltage, and I_{on} increases when $V_{GS}^{T,n}$ increases. In the case of the SWCNT TFT, V_{th} shifts toward more positive voltage, and $|I_{on}|$ increases when $V_{GS}^{T,p}$ decreases. Figure 3c, d shows output characteristics of

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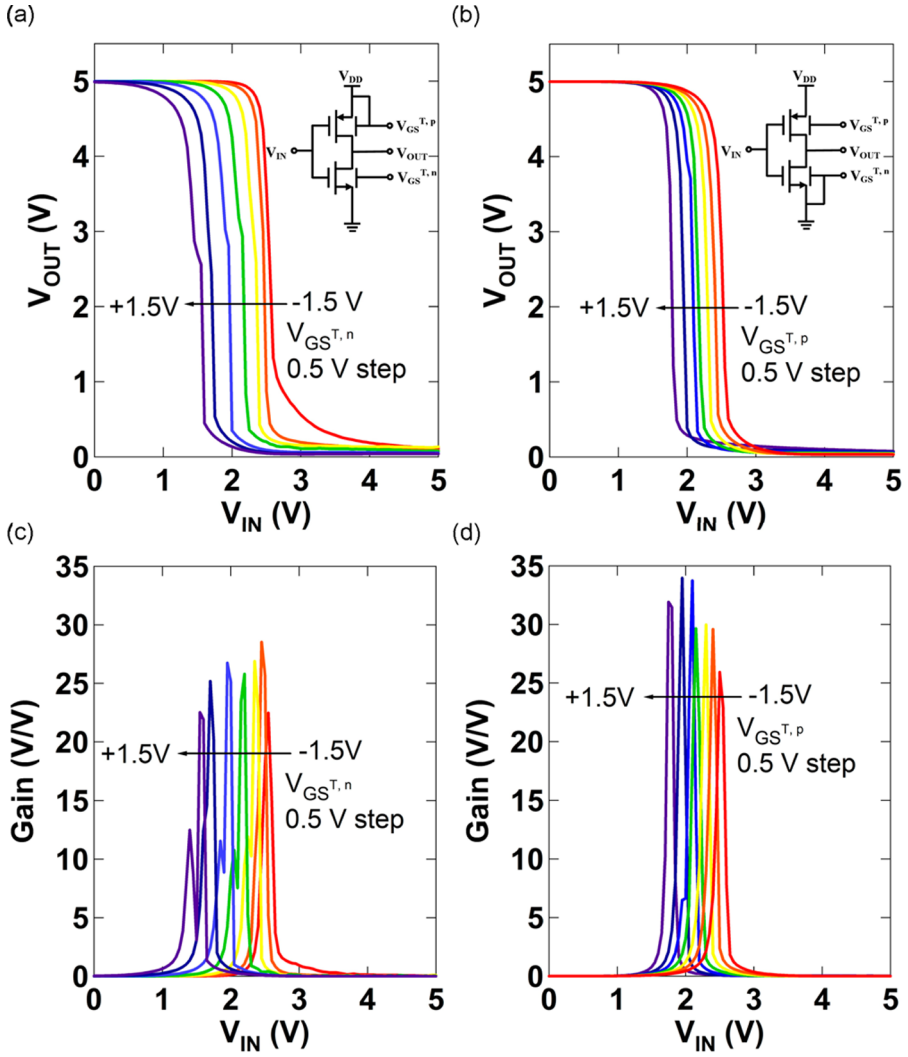

Figure 4. (a) Voltage transfer characteristics (VTCs) of the double-gate complementary inverter as a function of $V_{GS}^{T,n}$ and (inset) the top gate of p-TFT connected to the source (V_{DD}) of p-TFT. (b) VTCs of the double-gate complementary inverter as a function of $V_{GS}^{T,p}$ and (inset) the top gate of n-TFT connected to the source (GND) of n-TFT. (c) DC gains ($|dV_{out}/dV_{in}|$) of the inverter as a function of $V_{GS}^{T,n}$. (d) DC gains of the inverter as a function of $V_{GS}^{T,p}$.

the double-gate TFTs at both $V_{GS}^{T,p}$ and $V_{GS}^{T,n}$ = 1.5 V and at both $V_{GS}^{T,p}$ and $V_{GS}^{T,n}$ = −1.5 V, respectively. I_{DS} varies depending on V_{GS}^{T} for both TFTs; however, the difference in I_{DS} between when V_{GS}^{T} = 1.5 V and V_{GS}^{T} = −1.5 V is smaller in the SWCNT TFT compared to in the ZTO TFT. This difference can be attributed to the lower gate modulation of the SWCNT TFT in the saturation regime (Supporting Information, Figure S2). A possible reason for this is that the top gate dielectric stack is thicker for SWCNT TFTs compared to ZTO TFTs.

A complementary inverter was constructed by connecting double-gate SWCNT (p-channel) and ZTO (n-channel) TFTs as illustrated in Figure 2 and the insets of Figure 4a, b. The inverter was characterized by applying V_{GS}^{T} to either the top gate of the p-TFT or n-TFT, while the other top gate was connected to its source. Input voltages (V_{IN}) were applied to the connected bottom gate. Figure 4a shows voltage transfer characteristics of the inverter at different values of $V_{GS}^{T,n}$, where the curve shifts to the left along the axis of V_{IN} when $V_{GS}^{T,n}$ increases. This shift occurs because I_{DS} of the n-TFT increases with the increase of $V_{GS}^{T,n}$, while I_{DS} of the p-TFT remains the same. The DC gains ($|dV_{out}/dV_{in}|$) of the inverter at different $V_{GS}^{T,n}$ are shown in Figure 4c. The maximum gain point also shifts to the left when $V_{GS}^{T,n}$ increases. These shifts are observed similarly when $V_{GS}^{T,p}$ increases (Figure 4b, d). In this case, $|I_{DS}|$ of the p-TFT decreases with the increase of $V_{GS}^{T,p}$, while I_{DS} of the n-TFT remains the same. However, the shifts are less in magnitude in the SWCNT TFT case for the reason mentioned above.

The double-gate V_{th} tuning characteristics can be applied to ROSC circuits to control their oscillation frequencies. For example, five double-gate inverters were connected in a loop to construct a five-stage double-gate ROSC with a buffer stage as shown in Figure 5a. Figure 5b shows an optical micrograph of the ROSC. All TFTs in the ROSC circuit possess the same channel dimensions (L = 20 μm; W = 400 μm). Figure 5c, d shows output signals of the ROSC at three different values of $V_{GS}^{T,n}$ and $V_{GS}^{T,p}$, respectively, resulting in a frequency modulation of the ROSC. In particular, the oscillation frequency of the ROSC increases as $V_{GS}^{T,n}$ increases (Figure 5c). In contrast, the oscillation frequency of the ROSC decreases as $V_{GS}^{T,p}$ increases (Figure 5d).

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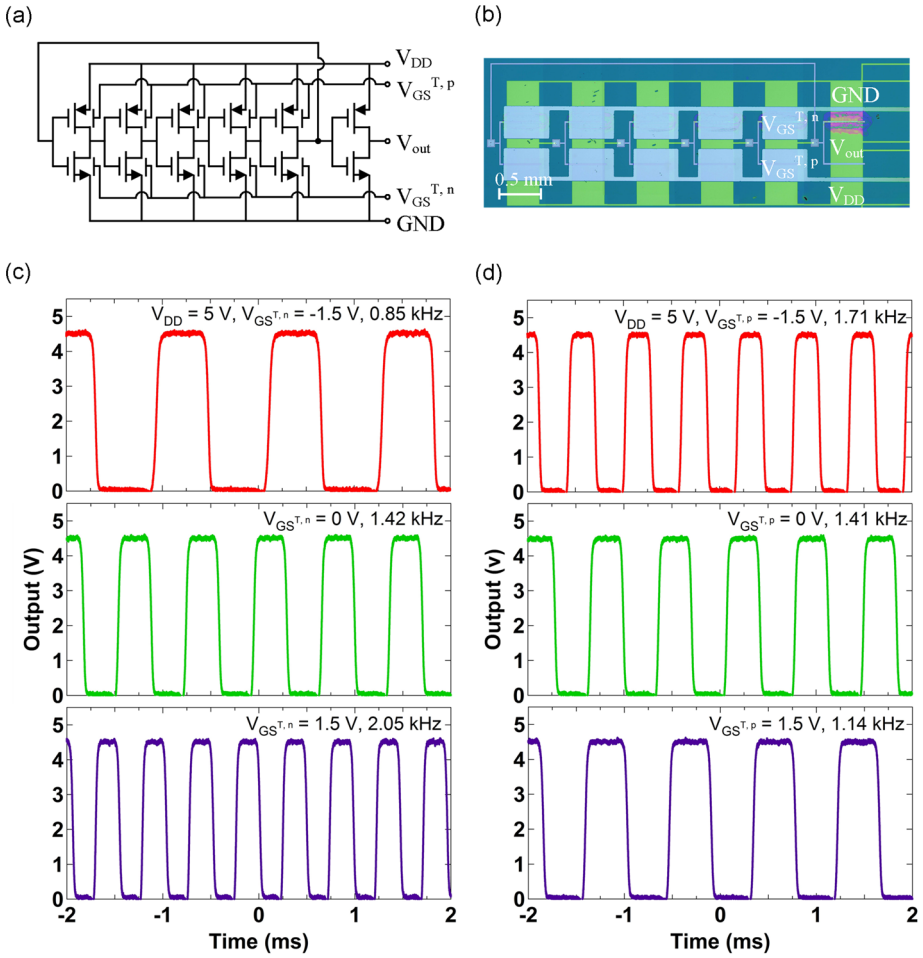

Figure 5. (a) Circuit diagram of a double-gate five-stage ROSC. (b) Optical micrograph of the double-gate five-stage ROSC; the upper six TFTs are ZTO (n-channel) TFTs, and the lower six TFTs are SWCNT (p-channel) TFTs. (c) Output signals of the double-gate ROSC at different values of $V_{GS}^{T,n}$ and (d) at different values of $V_{GS}^{T,P}$.

Figure 6 shows summarized tuning characteristics of the top gate potentials on TFTs, inverters, and ROSCs. Figure 6a shows the V_{th} tuning characteristics of the ZTO TFT by applying different values of $V_{GS}^{T,n}$, and Figure 6b shows the V_{th} tuning characteristics of the SWCNT TFT by applying different values of $V_{GS}^{T,P}$. The switching threshold of the inverter, where $V_{IN} = V_{OUT}$, decreases when $V_{GS}^{T,n}$ and $V_{GS}^{T,P}$ increase (Figure 6c, d).

The frequency of the ROSC increases linearly as $V_{GS}^{T,n}$ increases (Figure 6e), while the frequency decreases linearly as $V_{GS}^{T,P}$ increases (Figure 6f). Quantitatively, linear fitting curves almost exactly match the measured data points (R^2 = 0.999 in Figure 6e; R^2 = 0.997 in Figure 6f). This linearity is expected from the basic equation (eq 1) that describes the oscillation frequency in a CMOS-based ROSC:[32]

$$f \propto \frac{1}{NR_{on}C} \propto V_{ov} \quad (1)$$

where N is the number of stages, R_{on} is the on-resistance, C is the capacitance, and V_{ov} is the overdrive voltage ($V_{ov} = V_{GS} - V_{th}$). However, for TFTs with disordered semiconductors, R_{on} in eq 1 will change nonlinearly with the gate potential because of the dependence of mobility on carrier density. The capacitance, C, in eq 1 will also change in the opposite direction with the gate potential due to charge storage. The combined effect of both these changes results in a substantially linear oscillation frequency versus gate potential characteristic that we observe as shown in Figure 6e, f. Such a linear characteristic will result in minimal distortion of the analog signal. The frequency modulated square wave output of the VCRO will have a higher bandwidth (and hence sampling rate) compared to a conventional ADC,[5−7] in which the slow clock speeds of the organic- or printed-electronics-based digital electronics will limit performance. This improvement occurs because the oscillation frequencies of ROSCs are typically much higher than the clock frequencies of flip-flops or other digital components for any given technology.

CONCLUSION

A VCRO has been demonstrated by employing a double-gate structure where the active semiconductors of the circuits are deposited by inkjet printing. Threshold voltages in individual TFTs, switching thresholds in complementary inverters, and oscillation frequencies in ROSCs are systemically controlled by applying top-gate-source voltages in double-gated devices. A key requirement for the VCO, linearity between frequencies and voltages, has been achieved by simply adding a top gate dielectric and top gates on top of conventional ROSCs in place of more complex circuit designs. Consequently, the circuits demonstrated here are

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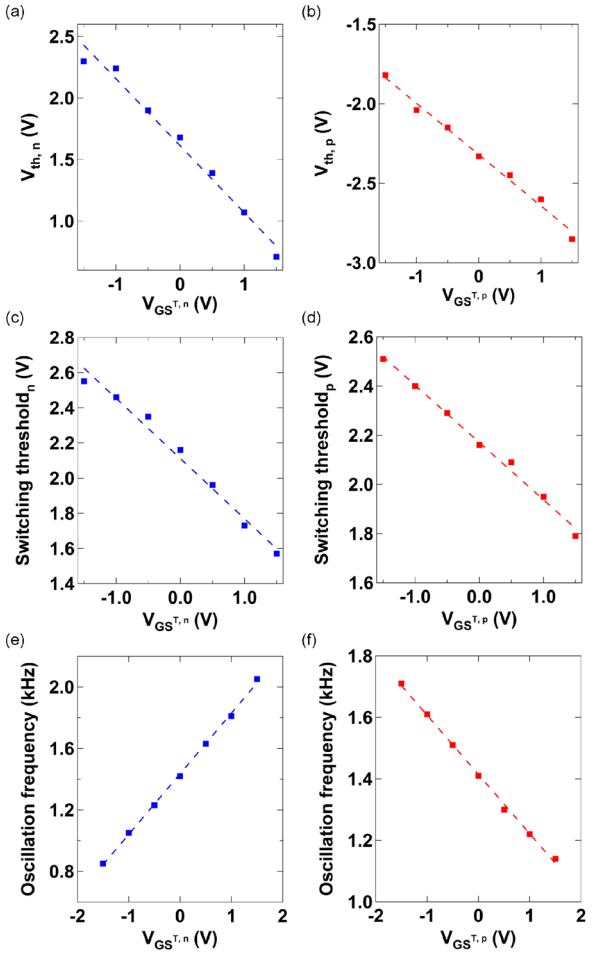

Figure 6. (a) Threshold voltage shift of the ZTO TFT as a function of $V_{GS}^{T,n}$. (b) Threshold voltage shift of the SWCNT TFT as a function of $V_{GS}^{T,p}$. (c) Switching threshold shifts of the inverter as a function of $V_{GS}^{T,n}$. (d) Switching threshold shifts of the inverter as a function of $V_{GS}^{T,p}$. (e) Oscillation frequencies of the double-gate ROSC as a function of $V_{GS}^{T,n}$ at V_{DD} = 5 V. (f) Oscillation frequencies of the double-gate ROSC as a function of $V_{GS}^{T,p}$ at V_{DD} = 5 V. Dotted lines in a–e show linear fitting of the measured data (shown in squares).

likely to accelerate efforts to realize printed-electronics-based signal processing in distributed sensors and related technologies.

■ ASSOCIATED CONTENT

Supporting Information

Capacitance of a bilayer of P(VDF-TrFE)/Al_2O_3; transfer characteristics of SWCNT and ZTO TFTs in the saturation regime; SPICE simulation results of double-gate inverters; propagation delay per stage of the double-gate ROSC as a function of top gate-source voltages. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.5b02093.

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Notes

The authors declare no competing financial interest.

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